the first information.

8. (Amended) The data processing system according to claim 4, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the data processing device controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent burst operations.

Please add the following new claims:

12. The data processing system according to claim 5, wherein the data processing device performs control in which data acquired in the burst operations for the single or plurality of times is filled in the cache memory according to the first information.

13. The data processing system according to claim 5, wherein in cache fill operations, the data processing device generates a synchronization signal synchronous with a delimiter of data axquired from the memory in the burst operations, and the data processing device generates a cache fill address for determining a data order of cache fill in synchronism with the synchronization signal in order to perform write control for the cache memory starting from the address information in a range of a burst length meat by the first information.

14. The data processing system according to claim 5, wherein in having access to a memory in a plurality of burst operations in response to a cache mishit, the data processing device controls a burst operation starting from a data location at an address in the cache mishit in a first burst operation, and the data processing device controls a burst operation starting from a top boundary of a data block defined by the burst length in subsequent burst operations.